Claims

What is claimed:

1. An interface apparatus in an image processing system, comprising:

an image sensor sensing an image;

an image processor processing the sensed image to output image data; and

a sensor interface coupled between the image sensor and the image processor, the sensor interface comprising,

a sensor type register storing information about the image sensor,

a micom storing the information in the sensor type register to control the image sensor, and

a sensor signal processor receiving signals corresponding to the sensed image from the image sensor, converting the signals into modified signals, which the image processor processes to output the image data, according to the information stored in the sensor type register, and transmitting the modified signals to the image processor.

2. The interface apparatus of claim 1, wherein the signals comprise a vertical synchronization signal, a horizontal synchronization signal, a pixel clock signal, and pixel data.

3. The interface apparatus of claim 1, wherein the information stored in the sensor type register comprises:

polarity information of the vertical synchronization signal, the horizontal synchronization signal, and the

pixel clock signal;

image signal processing (ISP) mode information and pattern signal information of the image processor;

horizontal size information of the sensed image; and

vertical size information of the sensed image.

4. The interface apparatus of claim 1, wherein the sensor type register comprises:

a sensor signal register;

a horizontal size register; and

a vertical size register.

5. The interface apparatus of claim 4, wherein:

the signals comprises a vertical synchronization signal, a horizontal synchronization signal, and a pixel clock signal;

the information comprises polarity information of the vertical synchronization signal, the horizontal synchronization signal, and the pixel clock signal, image signal processing (ISP) mode information of the image processor, horizontal size information of the sensed image, and vertical size information of the sensed image;

the sensor signal register stores the polarity information and the image signal processing (ISP) mode information;

the horizontal size register stores the horizontal size information; and

the vertical size register storing the vertical size information.

6. The interface apparatus of claim 1, wherein:

the signals comprises a vertical synchronization signal, a horizontal synchronization signal, a pixel clock

signal, and a pixel data signal;

the information comprises polarity information of the vertical synchronization signal, the horizontal synchronization signal, and the pixel clock signal, image signal processing (ISP) mode information of the image processor, horizontal size information of the sensed image, and vertical size information of the sensed image; and

the sensor signal processor comprises:

a first multiplexer inverting or non-inverting a polarity of the vertical synchronization signal transmitted from the image sensor according to the polarity information of the vertical synchronization signal stored in the sensor type register,

a second multiplexer outputting an output of the first multiplexer or a low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor,

a third multiplexer inverting or non-inverting a polarity of the horizontal synchronization signal transmitted from the image sensor according to the polarity information of the horizontal synchronization signal stored in the sensor type register,

a fourth multiplexer outputting an output of the third multiplexer or the low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor,

a fifth multiplexer inverting or non-inverting a polarity of the pixel clock signal transmitted from the image sensor according to the polarity information of the pixel clock signal stored in the sensor type register,

a sixth multiplexer outputting an output of the fifth multiplexer or the low state signal to the image processor according to the image signal processing (ISP)

mode information of the image processor, and

a seventh multiplexer outputting the pixel data signal or the low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor.

7. The interface apparatus of claim 1, wherein the micom communicates with the image sensor using a general purpose input/ouput signal transmitted between the micom and the image sensor.

8. An interface method of interfacing an image sensor and an image processor in an image processing system, the interface method comprising:

storing information about the image sensor in a sensor type register;

receiving signals from the image sensor;

converting the signals outputted from the image sensor into image data according to the information stored in the sensor type register; and

transmitting the converted image data to the image processor.

9. The interface method of claim 8, wherein the signals comprise a vertical synchronization signal, a horizontal synchronization signal, a pixel clock signal, and pixel data.

10. The interface method of claim 8, wherein the information stored in the sensor type register comprises:

polarity information of the vertical synchronization signal, the horizontal synchronization signal, and the pixel clock signal;

image signal processing (ISP) mode information and pattern signal information of the image processor;

horizontal size information of the sensed image; and

vertical size information of the sensed image.

11. The interface method of claim 8, wherein the sensor type register comprises:

a sensor signal register;

a horizontal size register; and

a vertical size register.

12. The interface method of claim 11, wherein:

the signals comprises a vertical synchronization signal, a horizontal synchronization signal, and a pixel clock signal;

the information comprises polarity information of the vertical synchronization signal, the horizontal synchronization signal, and the pixel clock signal, image signal processing (ISP) mode information and pattern signal information of the image processor, horizontal size information of the sensed image, and vertical size information of the sensed image; and

the storing of the information about an image sensor in a sensor type register comprises,

storing the polarity information and the image signal processing (ISP) mode information in the sensor signal register,

storing the horizontal size information in the horizontal size register, and

storing the vertical size information in the vertical size register.

13. The interface method of claim 8, wherein:

the signals comprises a vertical synchronization signal, a horizontal synchronization signal, and a pixel clock signal;

the information comprises polarity information of the vertical synchronization signal, the horizontal synchronization signal, and the pixel clock signal, image signal processing (ISP) mode information and pattern signal information of the image processor, horizontal size information of the sensed image, and vertical size information of the sensed image; and

the converting of the signals outputted from the image sensor into the image data according to the information stored in the sensor type register comprises,

inverting or non-inverting a polarity of the vertical synchronization signal transmitted from the image sensor according to the polarity information of the vertical synchronization signal stored in the sensor type register,

outputting the inverted or non-inverted vertical synchronization signal or a low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor,

inverting or non-inverting a polarity of the horizontal synchronization signal transmitted from the image sensor according to the polarity information of the horizontal synchronization signal stored in the sensor type register,

outputting the inverted or non-inverted horizontal synchronization signal or the low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor,

inverting or non-inverting a polarity of the pixel clock signal transmitted from the image sensor

according to the polarity information of the pixel clock signal stored in the sensor type register,

outputting the inverted or non-inverted pixel clock signal or the low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor, and

outputting the pixel data signal or the low state signal to the image processor according to the image signal processing (ISP) mode information of the image processor.